What is claimed is:

1. A bus interface extender used to increase an amount of bus devices that can be controlled by a bus arbitrator, wherein the bus arbitrator includes a plurality of first pins, and each of the first pins can be electrically coupled to a corresponding first bus device, so the bus arbitrator arbitrates request signals asking for use of a bus channel sent by the first bus devices, the bus interface extender including:

a plurality of second pins; and

at least one third pin, wherein the at least one third pin is electrically coupled to a corresponding one of the first pins of the bus arbitrator, and each of the second pins can be electrically coupled to a corresponding second bus device, so the bus interface extender arbitrates each request signal sent by each second bus device through the second pins asking for use of a bus channel, according to a first grant signal, that allows the use of the bus channel and is produced after arbitrating by the bus arbitrator and received by the bus interface extender through the at least one third pin.

2. The bus interface extender according to claim 1, further comprising:

a priority decision module for determining a priority sequence in using the bus channel for each second bus device according to a priority decision rule;

a grant decision module for deciding one of the second bus devices with the highest priority according to the priority decision rule and confirming whether the second bus device with the highest priority is in request status; and

a bus signal processing module for correspondingly sending a second grant signal to a proper one of the second bus device according to the first grant signal and a decision result decided by the grant decision module to form signal transmission between the proper one of the second bus device and a system bus.

3. The bus interface extender according to claim 2, wherein the priority decision rule uses a fixed-priority arbitration mode.

4. The bus interface extender according to claim 2, wherein the priority decision rule uses a round-robin priority arbitration mode.

5. The bus interface extender according to claim 1, wherein the bus arbitrator and the bus interface extender are installed in a PCI bus architecture.

6. The bus interface extender according to claim 1, wherein at least one of the second bus devices sends a request signal of asking use of the bus channel to the bus arbitrator through the at least one third pin of the bus interface extender, and the request signal asking for use of the bus channel is arbitrated by the bus arbitrator.

7. A bus interface extender used to electrically couple to a bus arbitrator to increase an amount of bus devices that can be controlled by the bus arbitrator, wherein at least one first bus device is coupled to the bus arbitrator directly, and at least one second bus device is electrically coupled to the bus interface extender, so that the bus arbitrator can arbitrate any request signals sent from each first bus device and each second bus device through the bus interface extender, the bus interface extender including:

a priority decision module for determining a priority sequence in using a bus channel for each the at least one second bus device according to a priority decision rule;

a grant decision module for deciding one of the at least one second bus device

with the highest priority according to the priority decision rule, and the at least one second bus device with the highest priority has sent a request signal; and

a bus signal processing module for correspondingly sending a second grant signal to the at least one second bus device with the highest priority according to the first grant signal and a decision result decided by the grant decision module to form signal transmission between the at least one second bus device with the highest priority and a system bus.

8. The bus interface extender according to claim 7, wherein the priority decision rule uses a fixed-priority arbitration mode.

9. The bus interface extender according to claim 7, wherein the priority decision rule uses a round-robin priority arbitration mode.

10. A bus interface extending method, using an extender to increase an amount of bus devices controllable by a bus arbitrator, wherein the bus arbitrator is electrically coupled to at least one first bus device directly, and the extender is electrically coupled to at least one second bus device, so that the bus arbitrator can arbitrate any request signals sent from each first bus device and each second bus device through the extender, bus interface extending method comprising:

receiving a first grant signal after arbitrating through the extender;

searching for one having the highest priority from the at least one second bus device according to a priority sequence of each second bus device predetermined in a priority decision rule, wherein the at least one second bus device with the highest priority has sent a request signal; and

sending a second grant signal to the at least one second bus device with the highest priority by the extender to grant access of forming a channel for controlling signal transmission between the at least one second bus device with the highest priority and a system bus.

11. The bus interface extending method according to claim 10, wherein the bus arbitrator is installed in a PCI bus architecture.

12. The bus interface extending method according to claim 10, wherein the priority decision rule uses a fixed-priority arbitration mode.

13. The bus interface extending method according to claim 10, wherein the priority decision rule uses a round-robin priority arbitration mode.

14. A bus system, electrically coupled to a plurality of first bus devices and a plurality of second bus devices, the bus system comprising:

a bus arbitrator coupled to the first bus devices and an extender for arbitrating a request signal sent by any of the first bus devices and the extender; and

the extender electrically coupled between the bus arbitrator and the second bus devices for transmitting a request signal sent by any of the second bus devices to the bus arbitrator for arbitrating, and when the extender receives a grant signal produced by the bus arbitrator after arbitrating, the extender transmits the grant signal to a proper one of the second bus devices according to a priority sequence and request status of the second bus devices, so as to form a signal transmission channel between the proper one of the second bus devices and a system bus.

15. The bus system according to claim 14, wherein the bus system is a PCI bus system.

16. The bus system according to claim 15, wherein the extender includes a memory medium and a circuit logic, the memory medium is used to store the priority sequence, and the circuit logic is used to determine grant of access to the grant signal to a corresponding one of the second bus devices according to the memory medium.

17. The bus system according to claim 16, wherein the circuit logic adjusts the priority sequence in the memory medium as each of the second bus devices is granted the grant signal.

18. A bus device extending method, comprising:

coupling a plurality of first bus devices to a bus arbitrator;

coupling a plurality of second bus devices to an extender;

coupling the extender to the bus arbitrator;

sending a first request signal from the extender to the bus arbitrator correspondingly when the extender receives a second request signal sent by the second bus devices; and

sending a second grant signal from the extender to a proper one of the second bus devices correspondingly according to a priority sequence of the second bus devices when the extender receives a first grant signal sent from the bus arbitrator.

19. The bus device extending method according to claim 18, wherein the priority

sequence of each second bus device is fixed.

20. The bus device extending method according to claim 18, wherein the priority sequence is changed and adjusted with a sequence when each second bus device is granted the second grant signal.

21. The bus device extending method according to claim 18, wherein the bus arbitrator is a PCI bus arbitrator.